



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20431
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10-063,212	03/29/2002	Robert L. Barry	BUR920010182	7089

28211 7590 03/28/2003

FREDERICK W. GIBB, III
MCGINN & GIBB, PLLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER

PHAM, LY D

ART UNIT PAPER NUMBER

2818

DATE MAILED: 03/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application

10/063,212

Applicant(s)

BARRY ET AL.

Examiner

Ly D Pham

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 14 January 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) 21-26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1-2,5-9,11-16,18-20 is/are rejected.
- 7) ☐ Claim(s) 3,10 and 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 29 March 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Claims 21 – 26 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim.

Election was made **without** traverse in Paper No. 5.

Drawings

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 – 2, 5 – 9, 11 – 16, 18 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Pat Pub 2002/0171101 A1).

Regarding **claims 1, 8, and 15**, Hsu et al. disclose a memory cell connected to true bitline and a complement bitline, said memory cell comprising:

a first transistor having a first drain (fig. 2, transistor 14); and a second transistor having a second drain (fig. 2, transistor 18), wherein said first drain is connected to said true bitline (transistor 14 with first drain connected to BL0—true bit line) and said second drain is connected to said complement bitline (transistor 18 with second drain connected to BL0'—complement bitline).

Although the memory structure shown by Hsu et al. is a flash type memory, nevertheless, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to realize its possible design for ROM type, as claimed, as read-only becomes another desirable and applicable arrangement (col. 5, paragraph 0062).

Regarding **claims 2, 9, and 16**, Hsu et al. also disclose the memory cell in claims 1, 8, and 15, wherein said first transistor further comprises a first source (source of first transistor 14), and said second transistor further comprises a second source (source of second transistor 18), and wherein a connection of one of said first source and said second source to a ground programs said ROM cell (fig. 2, one of the two transistors has its source connected to ground 30).

Regarding **claims 4 and 11**, the examiner takes an Official Notice that the claimed feature in these claims, namely, the connection of the memory cell in claim 2 comprises an electrical connection formed during manufacturing of said first and second transistors, is considered common and well known in the memory art, as memory chips are manufactured with processes including forming electrical connections (as part of metal layers) being well known in designs such as VLSI.

Regarding **claims 5, 12, and 18**, Hsu et al. further show the memory cell in claim 1, wherein both the gates of the first and second transistors are connected to a wordline (fig. 2, gates of transistors 14 and 18 are both connected to wordline WL0).

Regarding **claims 6, 13, and 19**, Hsu et al. also show the memory cell in claim 1, wherein said second transistor comprises a complement transistor to said first transistor (second transistor 18 is complement to first transistor 14).

Regarding **claims 7, 4, and 20**, Hsu et al. also show the memory cell in claim 1, wherein said memory cell shares said first drain and said second drain with corresponding drains of an adjacent memory cell in said array (in the memory array of fig. 2, drain of first transistor 14 shares the bitline BL0 with the adjacent transistor right below it and drain of second transistor 18 shares the bitline BL0' with the adjacent transistor right below it).

Allowable Subject Matter

5. Claims 3, 10, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Art Unit: 2818

7. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

9. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is 703-305-4862. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at 703-308-4910. The fax number for the organization where this application or proceeding is assigned is 703-308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham



March 21, 2003

HOAI HO
PRIMARY EXAMINER